

18

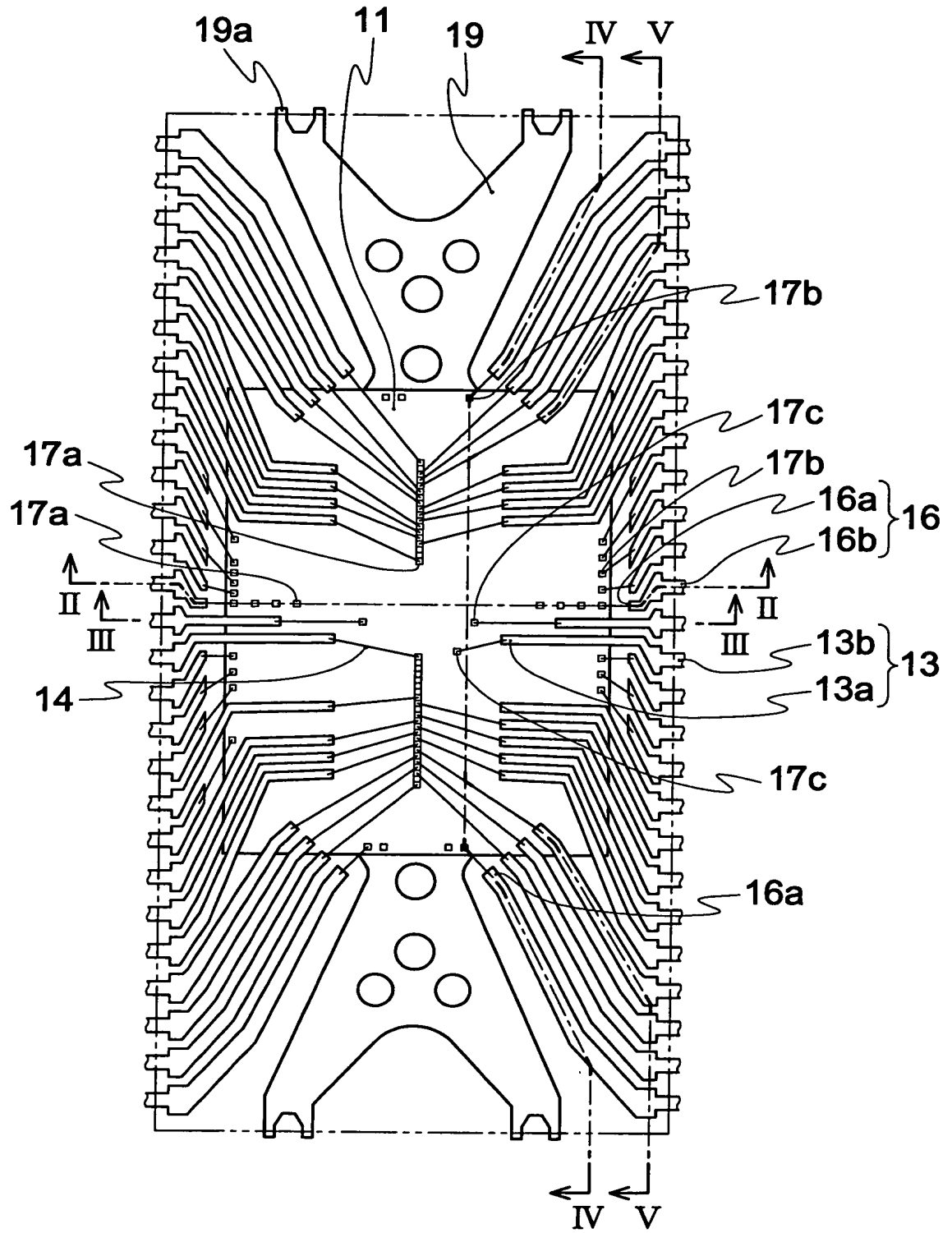


FIG. 2

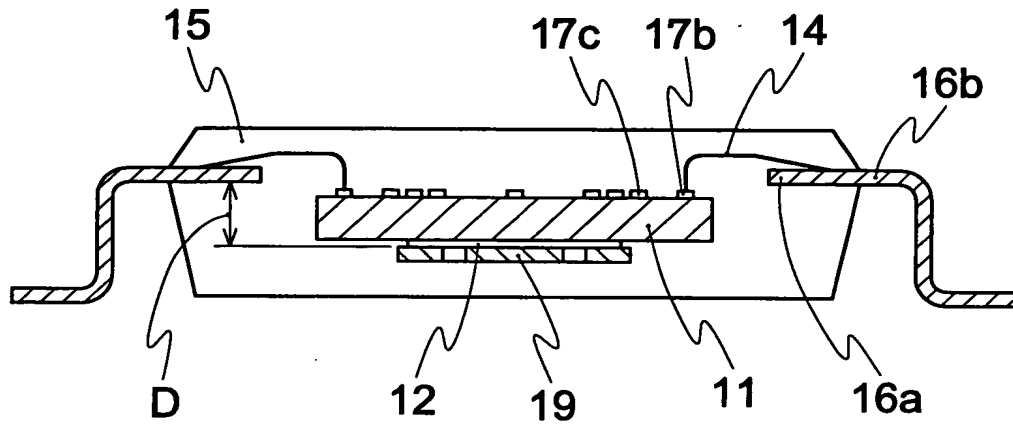


FIG. 3

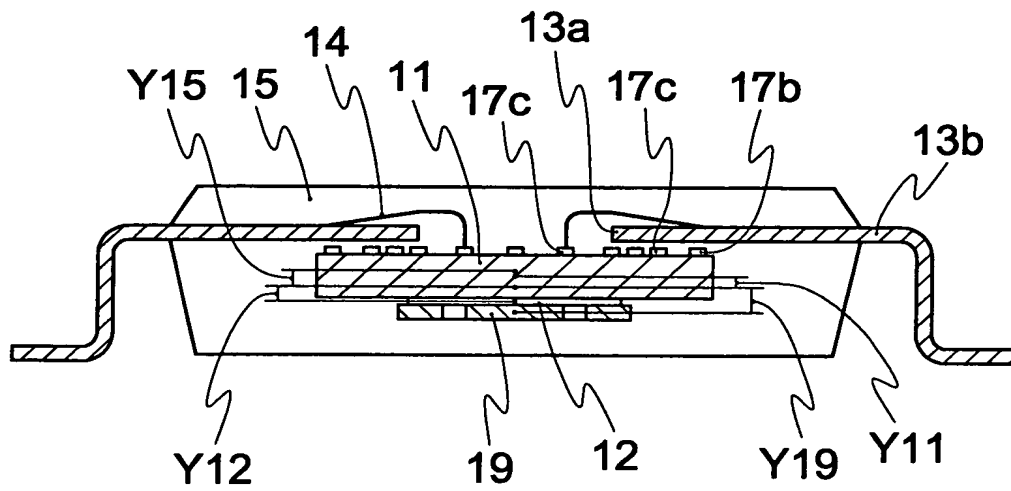


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 11. On the top surface of the substrate 11, there is a thin layer 12. A central region 19 is defined by a stack of layers: a hatched layer 17a, a dotted layer 17b, and a cross-hatched layer 17c. This central region 19 is flanked by two side regions 16a and 19a. The entire structure is covered by a top layer 19. A dimension line 'D' indicates the thickness of the substrate 11.

A cross-sectional view of a device. It features a central core with a hatched pattern, labeled 11. This core is surrounded by a layer labeled 12. On the left side, there are three distinct regions labeled 17a, 17b, and 17c, which appear to be part of a larger structure labeled 13a. The entire assembly is enclosed within a rectangular frame. At the bottom, there is a thin layer labeled 19, and at the very bottom, a thin layer labeled 19a. A dimension line labeled G indicates a specific width or thickness at the top of the device.

FIG. 6

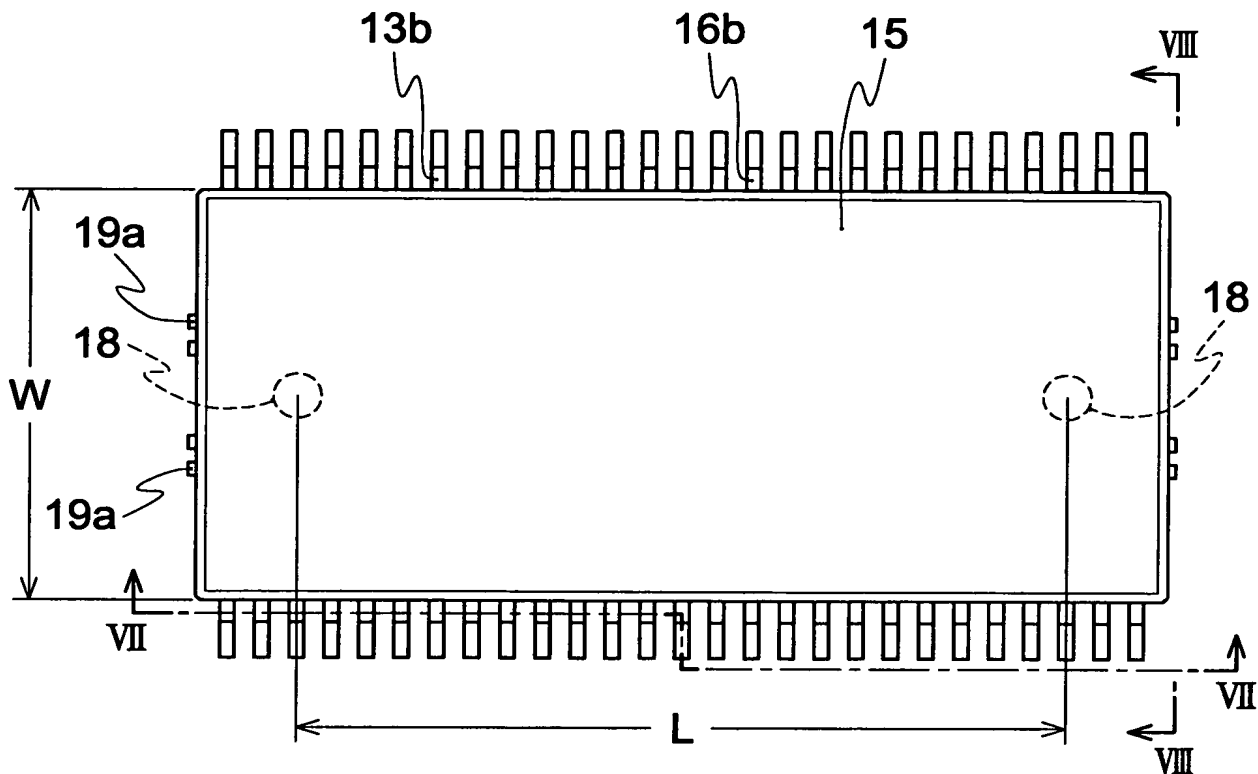


FIG. 7

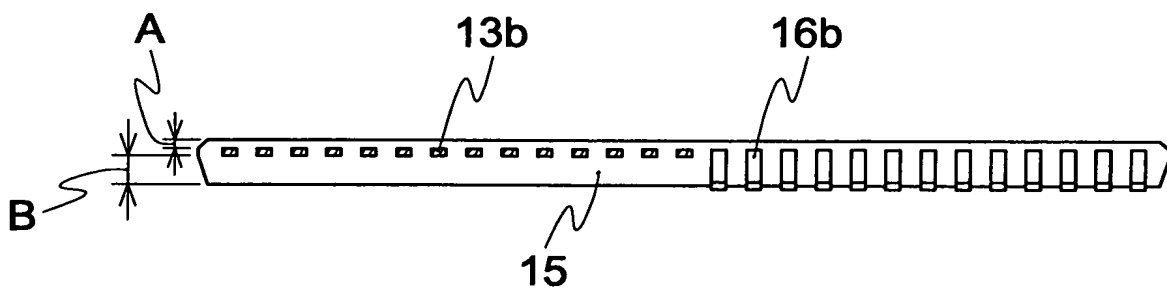


FIG. 8

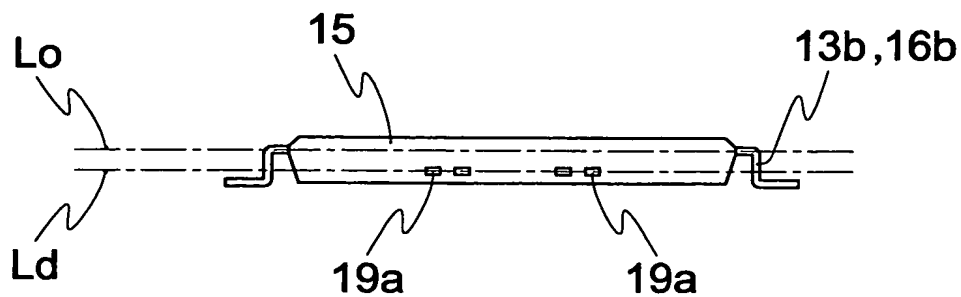


FIG. 9

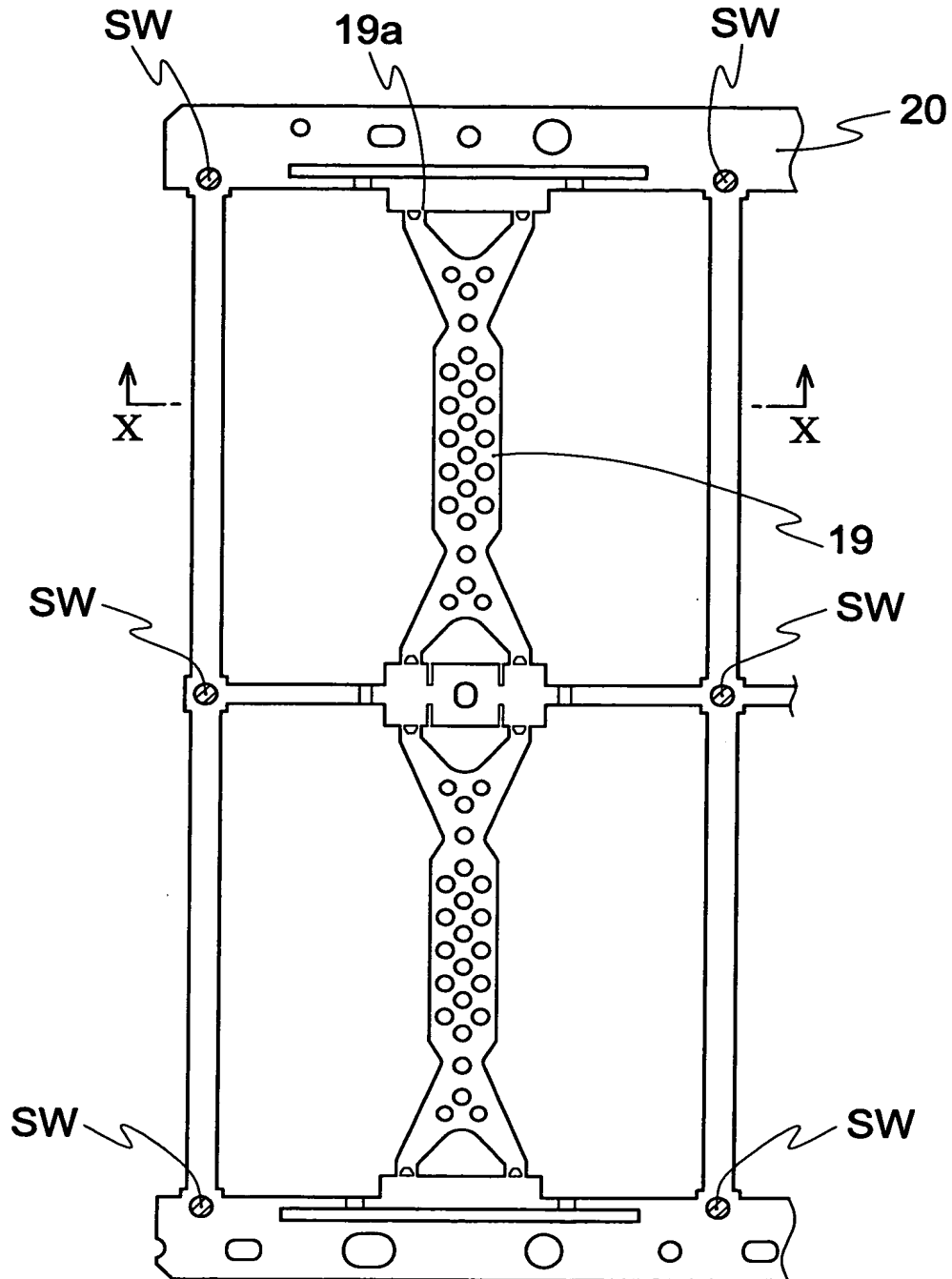


FIG. 10

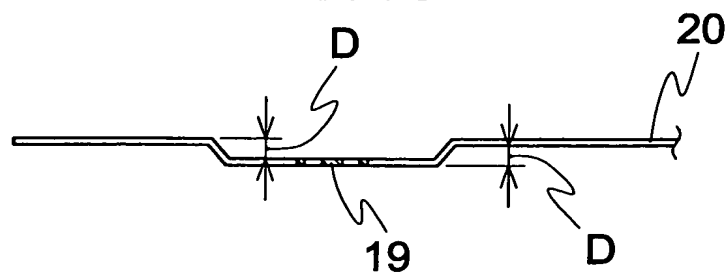


FIG. 11

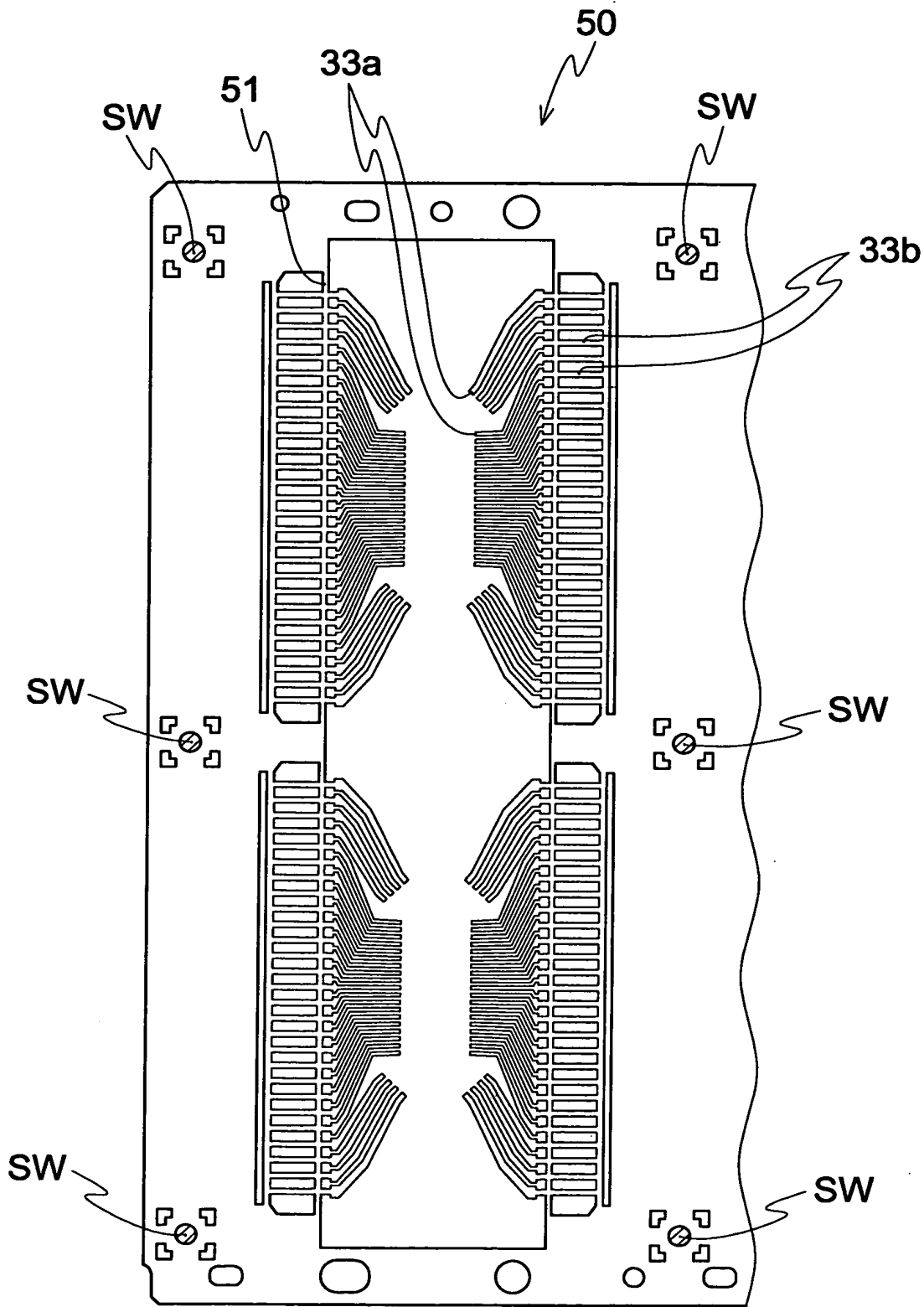


FIG. 11 is a schematic diagram of a semiconductor package 50. The package contains two vertical columns of semiconductor elements, 33a on the left and 33b on the right. Each column consists of multiple rows of elements connected by a network of conductive lines. The package is secured by four corner fasteners, each labeled "SW" and represented by a square with a circle and cross symbol. A label "51" points to a circular feature at the top center of the package. The entire assembly is enclosed in a rectangular frame with rounded corners.

FIG. 12

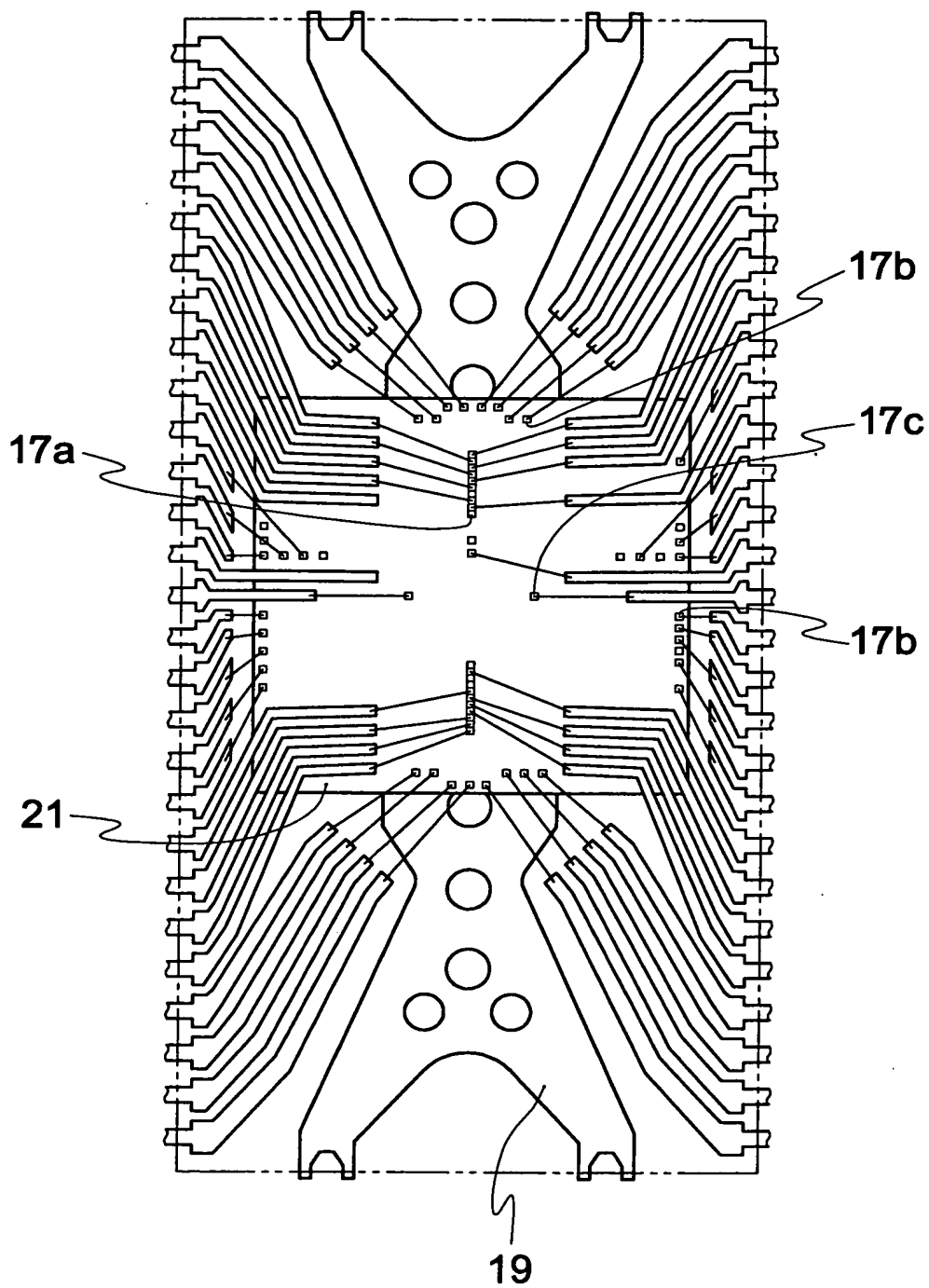


FIG. 13

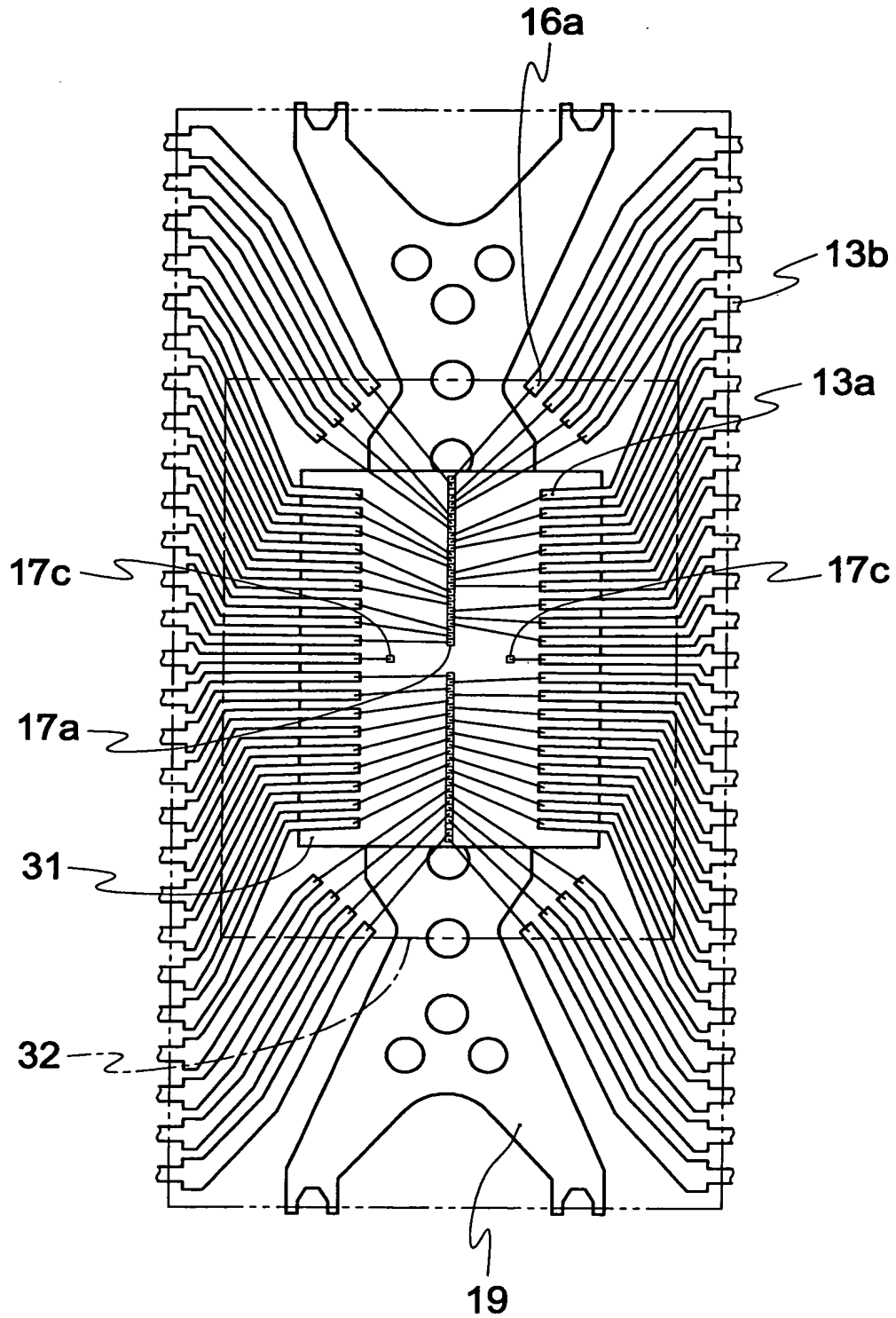




FIG. 14

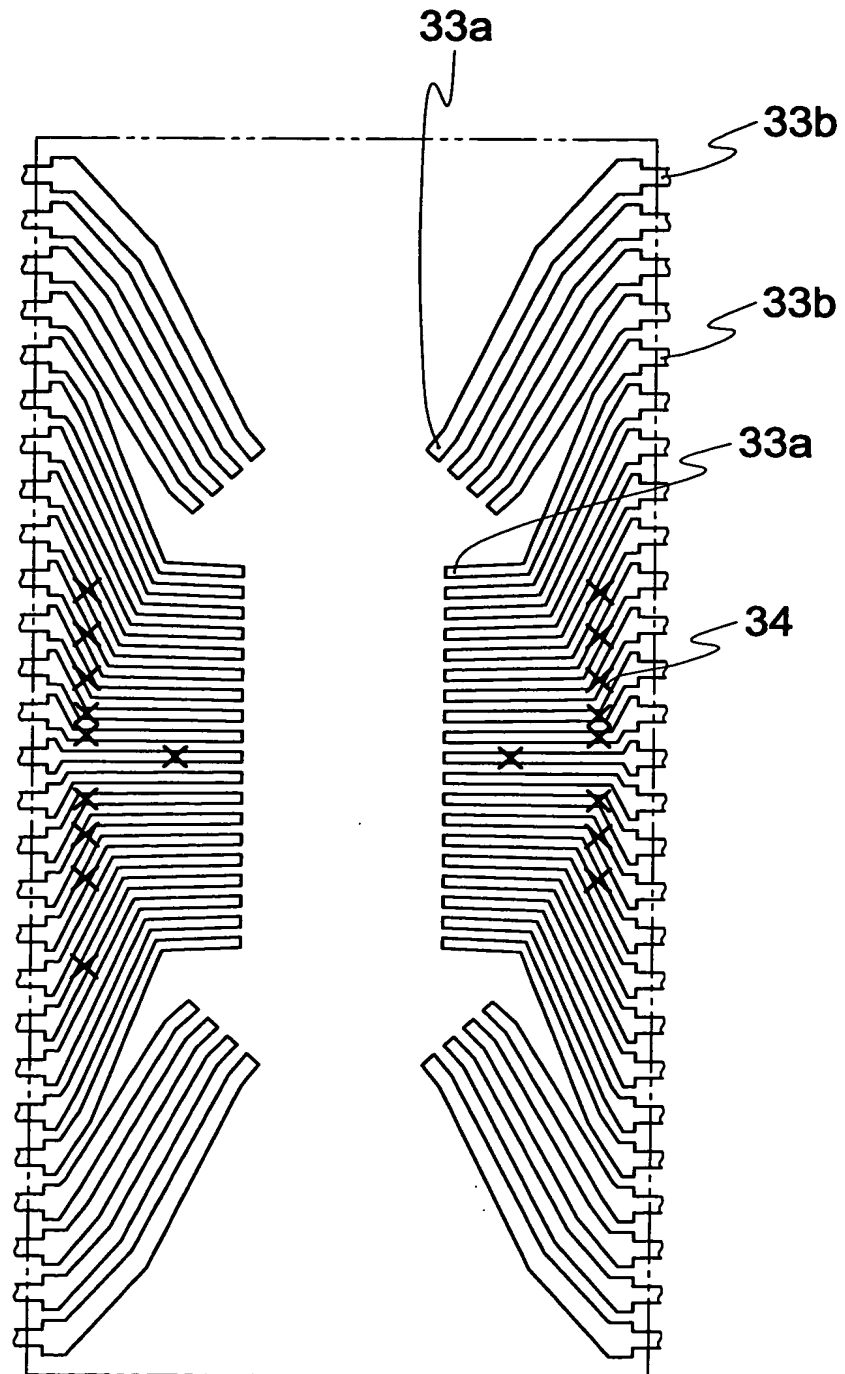


FIG. 15

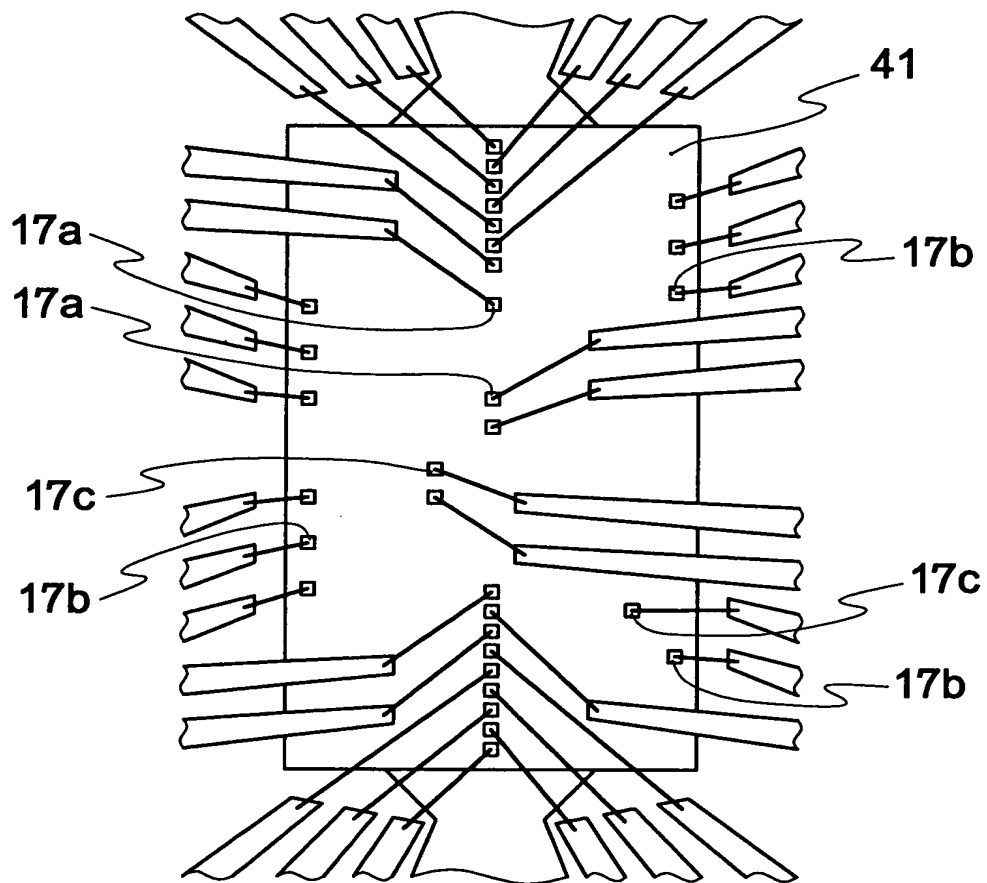


FIG. 16

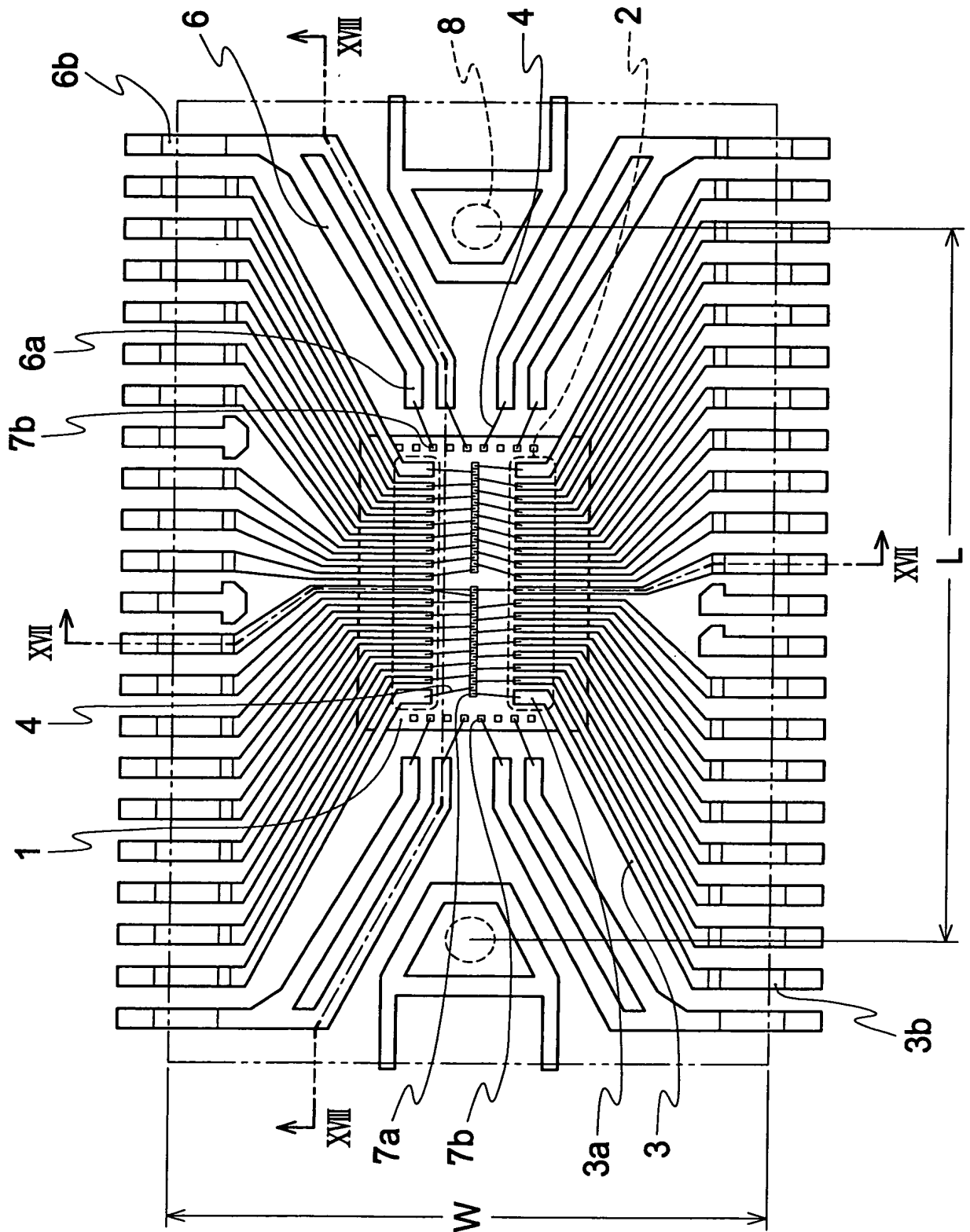


FIG. 18

